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Flexible High-Temperature MoS_2 Field-Effect Transistors and Logic Gates

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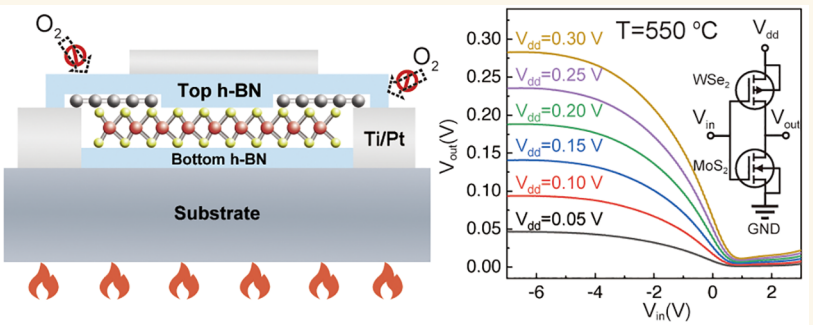

ABSTRACT: **High-temperature-resistant integrated circuits with excellent flexibility, a high integration level (nanoscale transistors), and low power consumption are highly desired in many fields, including aerospace. Compared with conventional SiC high-temperature transistors, transistors based on two-dimensional (2D) MoS_2 have advantages of superb flexibility, atomic scale, and ultralow power consumption. However, MoS_2 cannot survive at high temperature and drastically degrades above 200 °C. Here, we report MoS_2 field-effect transistors (FETs) with top/bottom hexagonal boron nitride (h-BN) encapsulation and graphene electrodes. With the protection of the h-BN/h-BN structure, the devices can survive at much higher temperature (≥500 °C in air) than those of the MoS_2 devices ever reported, which provides us an opportunity to explore the electrical properties and working mechanism of MoS_2 devices at high temperature. Unlike the relatively low-temperature situation, the on/off ratio and subthreshold swing of MoS_2 FETs show drastic variation at elevated temperature due to the injection of thermal emission carriers. Compared with metal electrode, devices with a graphene electrode demonstrate superior performance at high temperature (∼1-order-larger current on/off ratio, 3−7 times smaller subthreshold swing, and 5−9 times smaller threshold voltage shift). We further realize that the flexible CMOS NOT gate based on the above technique, and demonstrate logic computing at 550 °C. This work may stimulate the fundamental research of properties of 2D materials at high temperature, and also creates conditions for next-generation flexible harsh-environment-resistant integrated circuits.**

KEYWORDS: *MoS_2, high-temperature, field-effect transistor, graphene, flexible, logic gate*

Flexible nanoscale ultralow-power transistor capable of operating at high temperature is the building block for next-generation integrated circuits (ICs), which can operate in a harsh environment and can be deformed into arbitrary shapes as needed. They are highly desired in many fields, including aerospace, deep drilling, and robot for harsh environments.[1−3] Conventional high-temperature-resistant ICs are mainly based on silicon carbide (SiC) transistors.[4−7] For example, Elahipanah et al. reported a high-performance 4H-SiC bipolar junction transistor capable of operating at temperatures as high as 500 °C.[8] However, SiC transistors are rigid with relatively high power consumption, and they are difficult to reduce to the nanoscale.

Molybdenum disulfide (MoS_2), a layered 2D semiconductor, is capable of reaching one-atomic-layer thickness by mechanical exfoliation and chemical vapor deposition. Recently, great interest has been focused on MoS_2 as a channel material for atomic-scale ultralow-power high-performance FETs due to its superb electrical properties[9−12] (high carrier mobility, ultralow

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1/f noise). With extraordinary mechanical properties (high fracture strain), MoS_2 is also a promising candidate for flexible devices.[13−16] Li et al. reported four-inch wafer-scale integrated flexible transistor and logic gate arrays based on monolayer MoS_2.[17] Nevertheless, it is challenging for MoS_2 devices to be applied in high-temperature environments. As the temperature reaches 200 °C, a large number of S vacancies will form on the surface of MoS_2, which will adsorb oxygen molecules and result in doping of the material, leading to instability of the electrical properties.[18,19] At higher temperatures (>300 °C), MoS_2 will oxidize, with oxide pits appearing on its surface, and even drastically decompose.[20−22] The high-temperature-induced defects are detrimental to the electrical properties of MoS_2 devices.[23] As a result, the electrical properties and working mechanism of intrinsic MoS_2 devices at ultrahigh temperature are still unexplored, and the high-temperature MoS_2 FETs reported can only survive at relatively low temperatures (usually ≤350 °C) for very short times[24−33] (~70 s), as shown in Table 1. Bao et al. measured the photoelectric response of

Table 1. Comparison of High-Temperature MoS_2 Devices

thickness of MoS_2	device type	temperature tolerance	heating duration	ref
multilayer	FET	223 °C	\	24
monolayer	FET	173 °C	~12 s	25
multilayer	FET	175 °C	\	26
multilayer	TFT	223 °C	\	27
multilayer	TFT	107 °C	\	28
monolayer	synaptic transistor	350 °C	~70 s	29
few layer	photodetector	200 °C	\	30
monolayer	FET	125 °C	\	31
nanosheets	photodetector	300 °C	~70 s	32
multilayer	FET	107 °C	\	33
multilayer	FET	≥500 °C	>10 min	this work

bare MoS_2 channel transistors at 300 °C, but the operating time was only ~60 s. In addition, the real-time transfer characteristics of MoS_2 transistors at 300 °C was not investigated.[32] Seok et al. reported MoS_2 transistors, which can operate at 107 °C by using an Al_2O_3 protection layer grown by atomic layer deposition (ALD) on the MoS_2 surface.[33] There remains a deficiency in two-dimensional (2D) transition-metal dichalcogenide (TMD) devices capable of exhibiting stable operation as well as good performance at high temperatures.

Here, we present MoS_2 FETs with h-BN encapsulation and graphene electrodes, which can survive at a much higher temperature (≥500 °C in air) than those of high-temperature MoS_2 devices reported. The electrical characteristics and working mechanism of the MoS_2 FET under high temperature were comprehensively investigated. Compared with conventional metal electrodes, graphene electrodes effectively enhanced the high-temperature performance of the MoS_2 FETs (on/off ratio, subthreshold swing, and threshold voltage stability). Finally, we realized flexible high-temperature CMOS NOT gates based on the MoS_2 FET and WSe_2 FET with h-BN encapsulation and graphene electrodes and demonstrated logic computing at 550 °C.

RESULTS AND DISCUSSION

We fabricated MoS_2 FETs by mechanically stacking the bottom h-BN layer, multilayer MoS_2, graphene electrodes, and top h-BN layer sequentially on Si/SiO_2 substrate, followed by photolithography, metal deposition, and metal liftoff for top gate fabrication. The as-fabricated devices were annealed in Ar atmosphere at 200 °C for 2 h to remove the residues as well as to improve the MoS_2-graphene contact. The top and bottom h-BN form a heat-resistant encapsulation structure, as h-BN is a promising heat-resistant protection layer.[34,35] Additionally, the bottom h-BN layer eliminates the substrate scattering and significantly improves the electrical properties of MoS_2.[36] The top h-BN also serves as a gate dielectric layer. According to our previous work, h-BN demonstrated superb isolating properties, even at high temperature.[37] Figure 1c shows the optical microscopy image of a representative MoS_2 FET, which consists of five pieces of 2D-material flakes. Atomic force microscopy (AFM) measurements illustrate that the thicknesses of MoS_2 channel and graphene electrode are ~9.3 and ~9.8 nm, respectively (Figure 1d), and the thicknesses of top and bottom h-BN are ~35 and ~18 nm, respectively (Figure S1 in the Supporting Information). Raman spectrum of MoS_2 clearly shows characteristic peaks of E^1_{2g} (383 cm^{-1}) and A_{1g} (405 cm^{-1}) (Figure 1e).[38,39] Figure 1f demonstrates the Raman G peak (1580 cm^{-1}) and 2D peak (2721 cm^{-1}) of graphene,[40,41] and E_{2g} peak of h-BN (1364 cm^{-1}).[35] Sharp Raman peaks indicate the high quality of the 2D materials studied in this work. High-resolution transmission electron microscopy (HRTEM) cross-sectional image of the MoS_2 FET (Figure 1g) shows an atomically flat h-BN/graphene/MoS_2/h-BN heterostructure without defect or air gap, which is essential for high-temperature-resistant capability. The thickness of monolayer MoS_2 (0.65 nm) is consistent with reported values.[10,38]

High-temperature-resistant capability of the MoS_2 FET was investigated. The point defects and line defects in MoS_2 due to oxidation are difficult to be identified using an optical microscope. In addition, MoO_3, one of the typical oxides of MoS_2, sublimes easily at high temperature.[42] As a result, it is difficult to determine whether MoS_2 is oxidized during heating by observing the Raman peaks of MoO_3 (Figure S2 in the Supporting Information). We investigated the high-temperature-resistant capability of the devices by directly measuring their transfer curves at high temperature, inasmuch as the electrical properties are extremely sensitive to the defects/oxide in MoS_2.

We fabricated transistors with a bare MoS_2 channel and graphene electrodes on the bottom h-BN substrate as control groups (inset of Figure 2a). The transfer curve of a representative device measured at 25 °C is shown in Figure 2a, illustrating good electrical properties. Thereafter, the transfer curve of the same device was derived at 250 °C, which showed a clear rightward shift with increasing heating duration (Figure 2b). The rightward shift of transfer curve is caused by S vacancies generated on the MoS_2 surface as the temperature exceeds 200 °C (inset of Figure 2b). Oxygen molecules fill the S vacancies and result in a *p*-doping effect.[18,19,26] Under higher temperatures (500 °C), the transfer curve shifts rightward at first and then declines rapidly (Figure 2c). The optical microscopy image of the device after heating at 500 °C shows serious decomposition of the MoS_2 channel (Figure S3 in the Supporting Information) due to the water

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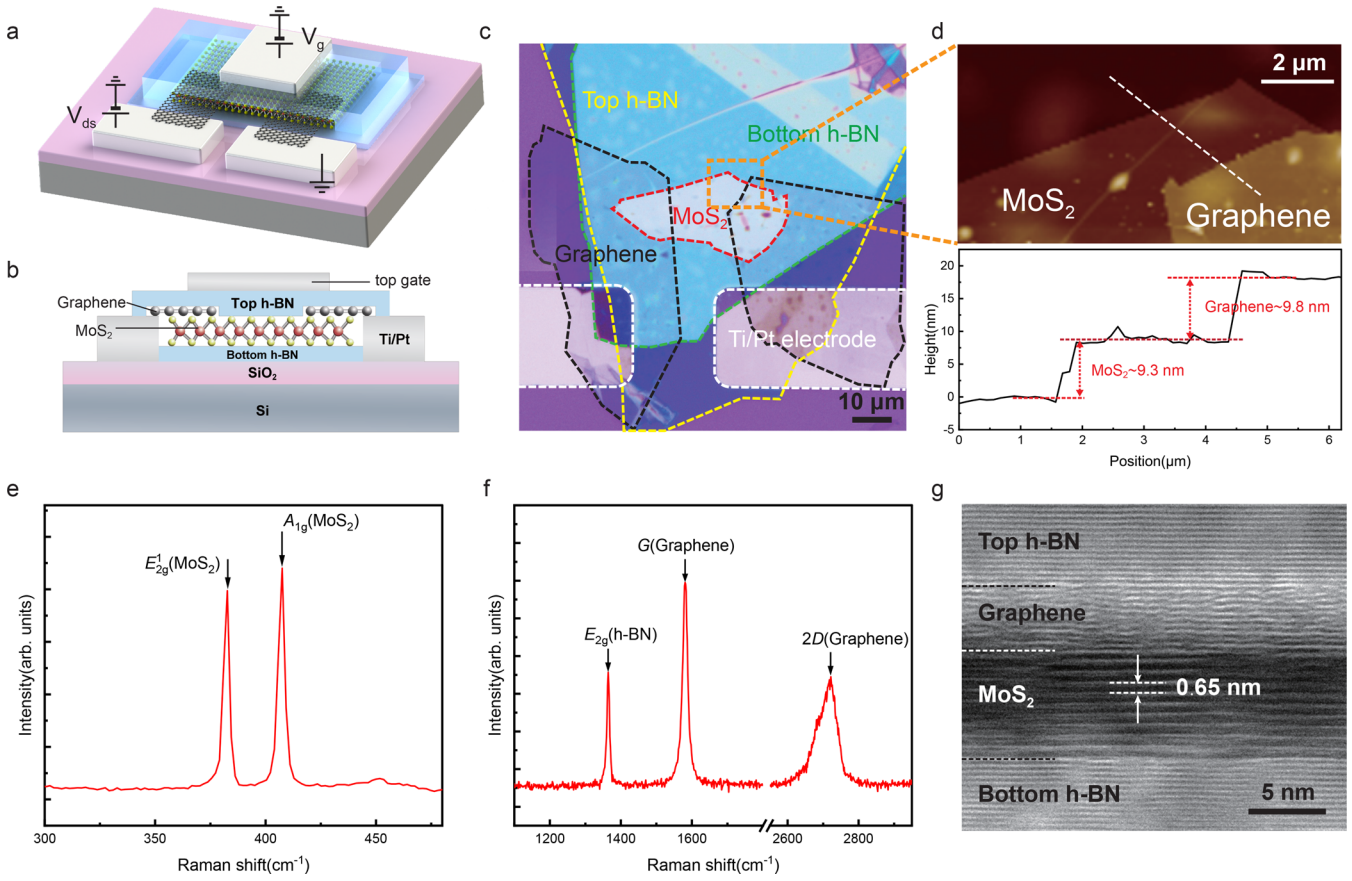

Figure 1. High-temperature-resistant MoS_2 FET. (a, b) Schematic views of MoS_2 FET with h-BN encapsulation and graphene electrodes. (c) Optical microscopy image of the MoS_2 device which consists of five pieces of 2D-material flakes. Dash lines indicate the edge of MoS_2 (red), graphene (black), bottom h-BN (green), and top h-BN (yellow). (d) AFM topographic image and height-position curve of MoS_2 and graphene electrode. (e, f) Raman spectra of MoS_2, h-BN and graphene. (g) HRTEM cross-sectional image of h-BN/graphene/MoS_2/h-BN heterostructure in the MoS_2 FET.

and oxygen in air (Figure S8 in the Supporting Information), which contributes to the decline of transfer curve. Therefore, bare MoS_2 can easily form S vacancies (at ∼250 °C) and even seriously decompose (at ∼500 °C) under high temperatures.

Dielectric deposited by atomic layer deposition (ALD) has been widely applied as the heat-resistant layer.[33] As control groups, we coated the MoS_2 channel with an ALD-deposited HfO_2 film with a thickness of 30 nm (inset of Figure 2d). The transfer curve of the device shows a similar rightward shift at 250 °C (Figure 2e), indicating the formation of S vacancies and O_2 doping. Under 500 °C, the transfer curve mainly shows a rightward shift without an obvious decline (Figure 2f). The optical microscope image of the device after heating at 500 °C demonstrates no serious decomposition of the MoS_2 (Figure S3). Therefore, the ALD-deposited dielectric layer can protect the MoS_2 channel from decomposition to some extent at high temperatures. But it cannot effectively prevent the formation of S vacancies and O_2 doping due to defects (pin holes, etc.) in the ALD-deposited film.[43−45] After annealing at 500 °C, the HfO_2 film on the metal electrode surface shows a large number of bubbles (Figure S4 in the Supporting Information), indicating the presence of defects in the ALD-deposited film.

As a comparison, the transfer curve of h-BN encapsulated devices demonstrated excellent stability without an obvious shift or decline, even at 500 °C (see Figures 2h and 2i). After heating to 500 °C, the MoS_2 film remained intact and no decomposition was observed by optical microscopy (Figure S3); yet, it still demonstrated good electrical properties (see Figures S11 and S12 in the Supporting Information). This is due to the high-quality h-BN crystal with extremely low defect density, as well as the atomically flat interfaces between the top and bottom h-BN layers, which play an important role in high-temperature protection by preventing the oxygen molecules from diffusing into the h-BN/h-BN encapsulation. As such, the h-BN/h-BN encapsulation effectively protects the MoS_2 channel under high temperature. As shown in Figure 2f, the initial transfer curve (t = 0 min, red curve) of the HfO_2 encapsulated device demonstrated a comparable I_{on}/I_{off} ratio (∼0.5) to that of the h-BN encapsulated device (Figure 2i). However, as the heating time increases, oxygen molecules fill the S vacancies on MoS_2 surface due to the poor protection of HfO_2 and result in the p-doping effect (Figure 2f). The significantly enhanced p-type conductivity leads to a relatively larger I_{on}/I_{off} ratio, which is unstable and uncontrollable. The h-BN encapsulated devices, on the other hand, are stable and maintain the intrinsic electrical properties of MoS_2 at high temperatures. In situ Raman spectra of h-BN encapsulated MoS_2 at different temperatures from 25 to 500 °C (Figure S9 in the Supporting Information) indicate that MoS_2 does not undergo structural phase transition at high temperatures. The temperature that our MoS_2 FETs can tolerate (≥500 °C) is much higher than those of the high-temperature MoS_2 devices reported (Table 1). It provides us the opportunity to explore

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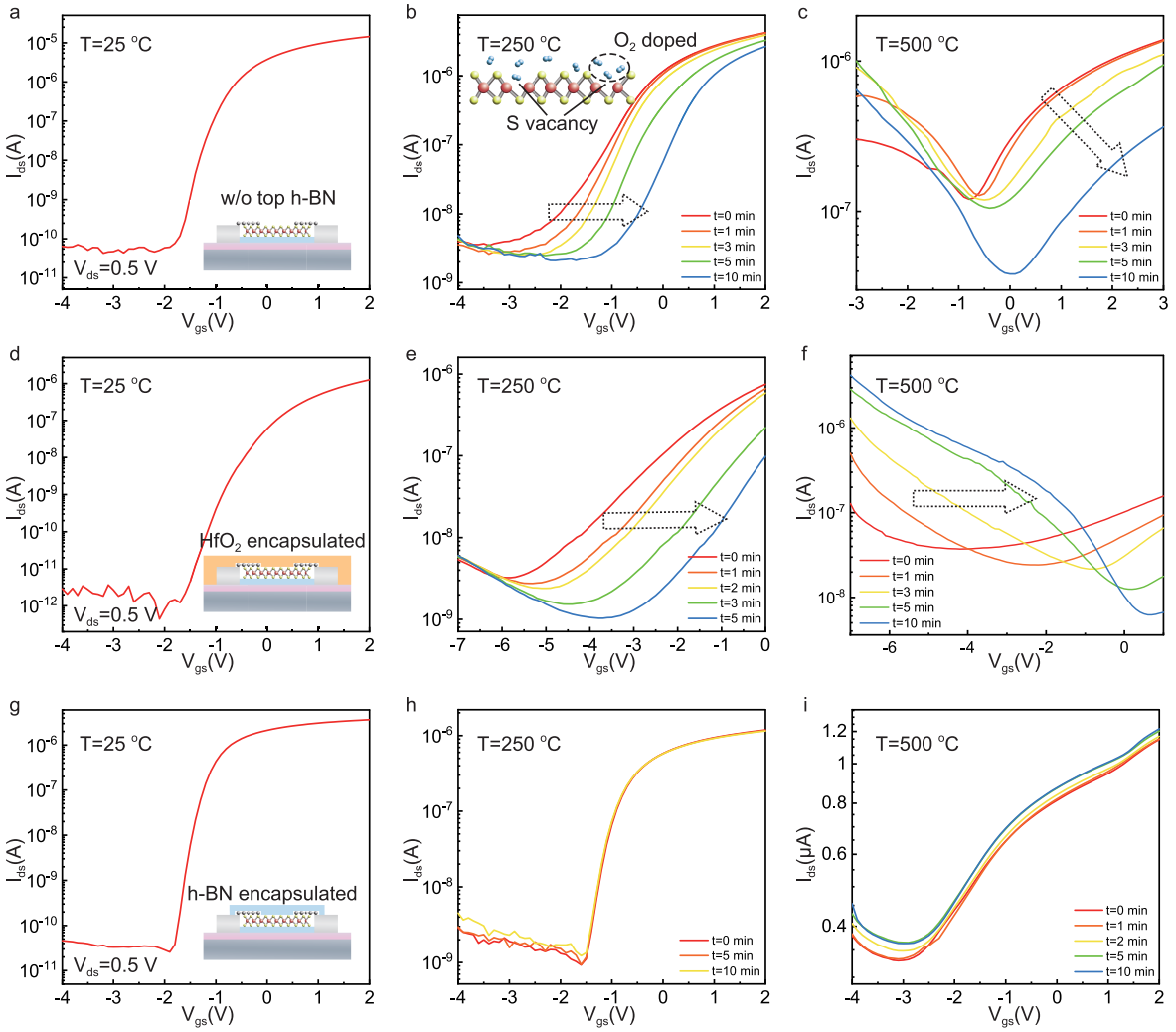

Figure 2. High-temperature-resistant capability. (a) Transfer curve of transistor with bare MoS_2 channel at 25 °C (V_{ds} = 0.5 V). The inset is the schematic of the device structure. (b, c) Transfer curves of the transistor with bare MoS_2 channel measured at 250 and 500 °C, respectively, with different heating duration. (d) Transfer curve of ALD HfO_2-coated MoS_2 FET at 25 °C. (e, f) Transfer curves of ALD HfO_2-coated MoS_2 FET measured at 250 and 500 °C, respectively, with different heating duration. (g) Transfer curve of h-BN encapsulated MoS_2 FET at 25 °C. (h, i) Transfer curves of h-BN encapsulated MoS_2 FET measured at 250 and 500 °C, respectively, with different heating durations.

the outstanding properties of MoS_2 under ultrahigh temperatures.

Temperature-dependent electrical properties of our MoS_2 FETs were then investigated. Previous studies mainly focus on relatively low-temperature situations (room temperature or below), and the electrical properties of MoS_2 at high temperature remain unexplored. Figure 3a shows the transfer curves measured as temperatures vary from −150 to 300 °C (source-drain voltage V_{ds} = 500 mV). The transfer curves demonstrate that the conductivity of the device increases with increasing temperature as the gate voltage V_{gs} is <0.4 V, while the conductivity decreases with increasing temperature as V_{gs} > 0.4 V, indicating the presence of metal−insulator-transition (MIT) phenomenon in the MoS_2 channel (MoS_2 exhibits an insulating behavior at V_{gs} < 0.4 V, and a metallic behavior at V_{gs} > 0.4 V; see Figure S5 in the Supporting Information). The Ioffe−Regel criterion predicts the existence of a MIT as the parameter $k_F \cdot l_e$ satisfies the criterion $k_F \cdot l_e \approx 1$, where k_F is the Fermi wave vector,

$$k_F = \sqrt{2\pi n_{2D}}$$

and l_e is the mean free path of electrons,

$$l_e = \frac{\hbar k_F \sigma}{n_{2D} e^2}$$

where n_{2D} is the charge density, $\hbar$ the reduced Plank constant, σ the sheet conductivity, and e the elementary charge).[12] For the MoS_2 device, the strong Coulomb interactions of MoS_2 caused by its relatively high effective mass and low dielectric constant contribute to the existence of MIT. A large gate voltage V_{gs} leads to $k_F \cdot l_e \gg 1$, resulting in the metallic phase, and a small V_{gs} leads to $k_F \cdot l_e \ll 1$, which results in the insulating phase. Previous studies reported MIT phenomenon at relatively low temperatures,[10,12,46] and our experiments show that this phenomenon also exists under high temperature. The observed MIT phenomenon indicates the barrier-free contact between graphene and MoS_2. Based on the thermionic emission theory, the drain current I_{ds} can be described by the following equation:[47,48]

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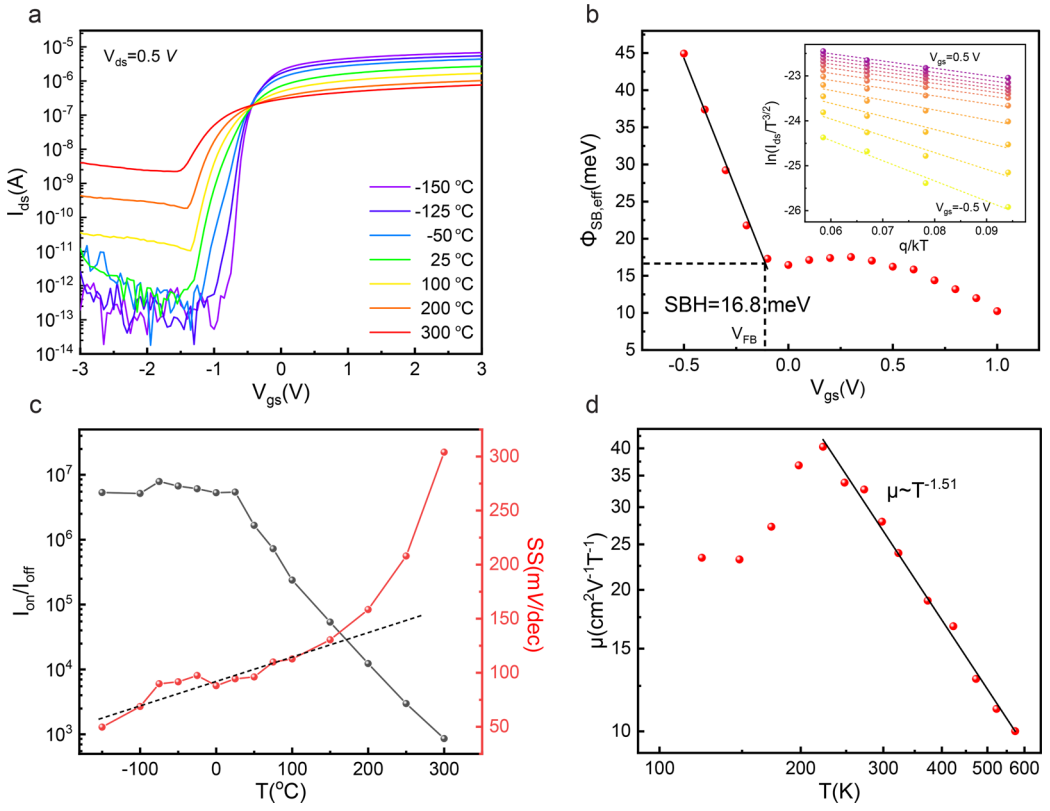

Figure 3. Temperature-dependent electrical properties of MoS_2 FET with h-BN encapsulation and graphene electrodes. (a) Transfer curves measured under different temperatures (V_{ds} = 0.5 V). (b) Effective Schottky barrier of the graphene-electrode device as a function of the gate voltage. Inset shows a linear-fitted Arrhenius plot as V_{gs} varies from −0.5 V to 0.5 V. (c) On/off ratio and SS derived under different temperatures. (d) Carrier mobility as a function of temperature.

$$I_{ds} = AA_{2D}^{*}T^{3/2}\exp\left[-\frac{q}{kT}\left(\phi_{SB,eff} - \frac{V_{ds}}{n}\right)\right] \quad (1)$$

where A is the channel area, A^* the Richardson constant, T the absolute temperature, k the Boltzmann constant, $\phi_{SB,eff}$ the effective Schottky barrier, and n the ideality factor. $\phi_{SB,eff}$ can be extracted from Arrhenius plots (see the inset of Figure 3b, $\ln(I_{ds}/T^{3/2})$ vs q/kT). Since the gate voltage V_{gs} is smaller than the flat band voltage V_{FB} ($V_{gs} < V_{FB}$), the extracted $\phi_{SB,eff}$ has a linear relationship with V_{gs} and gradually becomes sublinear as $V_{gs} > V_{FB}$.[49] Consequently, we extracted the Schottky barrier height (SBH) of 16.8 meV by finding the intersection of linear and sublinear regions (Figure 3b). The low SBH value implies that MoS_2/graphene interface has almost ohmic contact, because of the special band structure of graphene.[10,37] The contact resistance, which is another crucial parameter for high-quality contacts, varied from 4 to 46 kΩ μm and decreased as the temperature decreased and the gate voltage increased (see Figure S10 in the Supporting Information).

We systematically studied the effect of the high-temperature environment on the core parameters of the MoS_2 FETs. Figure 3c demonstrates the current on/off ratio of the device as a function of the temperature. The on/off ratio (~10^7) shows negligible change at low temperatures (<25 °C). At high temperatures, it largely decreases as temperature increases (~10^3 at 300 °C), and shows almost linear dependence on temperature. The reduction of on/off ratio is attributed to the enhancement of hot electron emission across the Schottky barrier at elevated temperature, which leads to a significant increase in the off-state current (Figure 3a).

Figure 3c shows the subthreshold swing (SS = $dV_{gs}/d\ln I_{ds}$) of the device as a function of the temperature. A small SS implies a strong gating effect. At relatively low temperatures (<100 °C), SS increases slowly and shows an almost linear dependence on temperature. SS increases rapidly above 100 °C. The SS of MoS_2 FET increases from 49.6 mV/dec at −150 °C to 304 mV/dec at 300 °C. According to eq 2,[50]

$$SS = \ln 10\left(\frac{kT}{q}\right)\left(\frac{C_{ox} + C_s}{C_{ox}}\right) \quad (2)$$

where C_{ox} is the dielectric capacitance and C_s is the depletion capacitance. Higher temperature T and larger C_s values lead to larger SS. At relatively low temperatures, SS is only affected by T, while at high temperatures, the injection of thermal emission carriers expands the width of the depletion region, and thus increases C_s. Therefore, the enhancement of both C_s and T is responsible for the rapid variation of SS at high temperatures.

The carrier mobility (μ) of MoS_2 is given by the following equation:[48]

$$\mu = \frac{dI_{ds}}{dV_{gs}}\left(\frac{L}{W}\right)\left(\frac{1}{C_{ox}V_{ds}}\right) \quad (3)$$

where L and W represent the channel length and width with $W/L \approx 1$, respectively. Figure 3d illustrates the carrier mobility of our MoS_2 device as a function of temperature on the logarithmic scale. The carrier mobility increases at first as the temperature increases and then μ starts to decrease from −50 °C (−223 K), with a maximum value of 42 $cm^2\ V^{-1}\ s^{-1}$. It has

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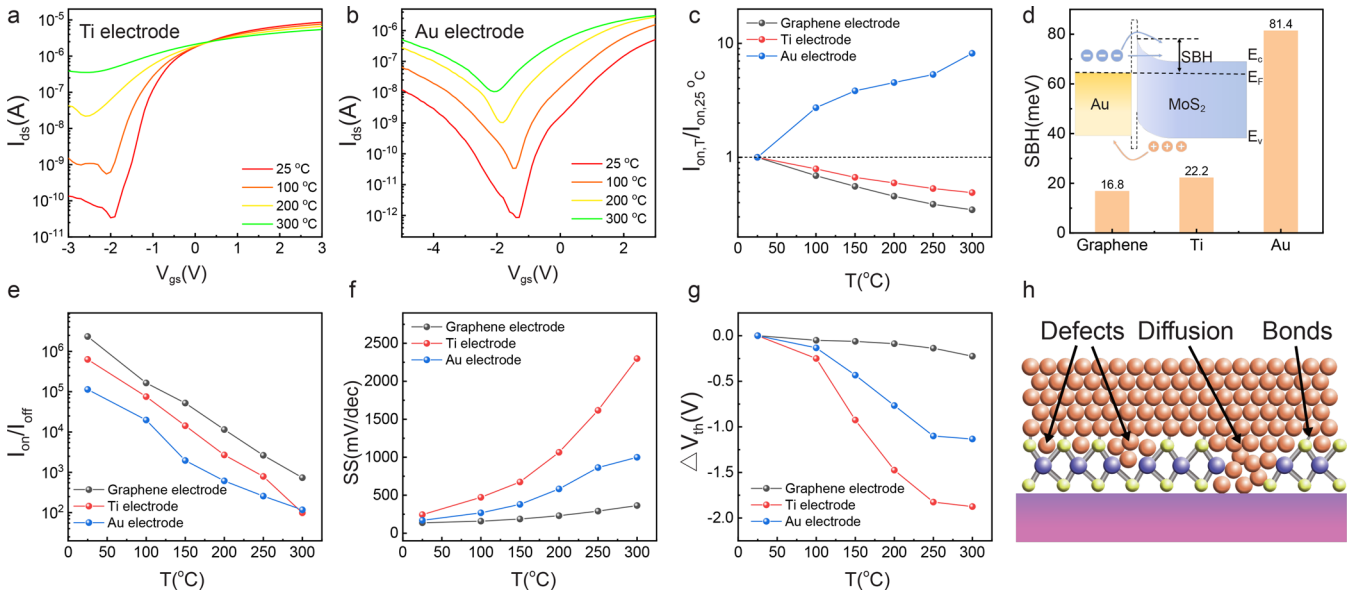

Figure 4. Comparison of graphene and metal electrodes at high temperatures. (a) Transfer curves of Ti-electrode MoS_2 FET measured under different temperatures (V_{ds} = 0.5 V). (b) Transfer curves of Au-electrode MoS_2 FET measured under different temperatures (V_{ds} = 0.5 V). (c) $I_{on,T}/I_{on,25\ °C}$ derived under different temperatures. $I_{on,T}$ is the on-state current under different temperatures, and $I_{on,25\ °C}$ is the on-state current at 25 °C. (d) Schottky barrier height (SBH) values of graphene-MoS_2, Ti-MoS_2, and Au-MoS_2, respectively. Inset shows the band diagram of Au-MoS_2 contact. (e, f, g) I_{on}/I_{off} ratio, SS, and ΔV_{th} of MoS_2 FETs with three types of electrodes derived under different temperatures. (h) Schematic of the metal/MoS_2 interface.

been reported that the carrier mobility fits the expression $\mu \sim T^{-\gamma}$, with the exponent being 1.26−1.74 for multilayer MoS_2, since carriers are limited by phonon scattering.[10,12,46] However, previous studies all focused on relatively low-temperature situations, and carrier transport properties in the MoS_2 film at high temperature have not been revealed. According to our experimental results, μ still fits the expression $\mu \sim T^{-\gamma}$ at high temperature, with an exponent of γ = 1.51, suggesting that the carriers in MoS_2 are still mainly limited by phonon scattering at high temperatures. Our study is important for understanding the carrier transport properties and mechanism in an atomically thin MoS_2 film at elevated temperatures.

To investigate the influence of electrodes to the high-temperature MoS_2 FETs, we prepared devices with Ti and Au electrodes, respectively, as control groups. Ti and Au are a typical small work function metal (4.3 eV) and a relatively large work function metal (5.1 eV), respectively,[47] which are widely used for MoS_2 FETs. As-fabricated devices were annealed in an Ar atmosphere at 200 °C to improve MoS_2-electrode contact properties. Figure 4a illustrates the transfer curves of a representative Ti-electrode device as the temperature varies from 25 °C to 300 °C. Drain current I_{ds} increases as the temperature rises for V_{gs} < 0.2 V, and decreases for V_{gs} > 0.2 V, indicating MIT phenomenon and low SBH in Ti-MoS_2 contact, similar to that of graphene-electrode MoS_2 FETs. Interestingly, Au-electrode devices did not exhibit MIT phenomenon (on-state current $I_{on,T}$ of Au-electrode device increases as the temperature increases, while $I_{on,T}$ of Ti- and graphene-electrode devices exhibit the opposite trend, Figures 4b and 4c), which may result from large SBH. The SBH of Au-MoS_2 contact we measured (81.4 meV) is larger than that of Ti-MoS_2 contact (22.2 meV), as shown in Figure 4d and Figure S6 in the Supporting Information, and the SBHs are consistent with reported values.[10,51,52] Graphene-MoS_2 has the lowest SBH (16.8 meV), implying superb contact properties. Additionally, Au-electrode devices show a strong bipolar character. This is because the barrier between metal and valence band top of MoS_2 is lower when MoS_2 is in contact with a large work function metal (Au) (inset of Figure 4d), thus more holes are injected across the barrier into the channel, leading to strong *p*-branches.[49]

Compared with metal electrodes, graphene-electrode devices with superb contact properties demonstrate much better high-temperature performance. Graphene-electrode MoS_2 FETs show ∼1 order of magnitude larger on/off ratio at elevated temperatures (Figure 4e). The SS values of MoS_2 FETs with different types of electrodes are comparable at room temperature. However, the SS of metal-electrode devices increases more significantly at high temperatures (3−7 times that of graphene-electrode devices at 300 °C, Figure 4f). As the temperature rises, the threshold voltage (V_{th}) of the MoS_2 FET has a leftward shift. Graphene-electrode devices demonstrate much smaller threshold voltage shift (ΔV_{th}) than those of metal-electrode ones (5−9 times smaller at 300 °C), indicating superior high-temperature stability of electrical properties, as shown in Figure 4g. It has been reported that covalent bonds, defects, interface diffusion, and atomic disorder may occur at the metal-MoS_2 interface,[49] as shown in Figure 4h. Additionally, Ti may react with MoS_2, especially at elevated temperature, forming Ti_xS_y and metallic Mo at the interface.[53] These factors weaken the electrical properties of the MoS_2-metal contact and result in more significantly change (degradation) of SS and ΔV_{th}. Graphene, on the other hand, is stable and difficult to form interface diffusion with or react with MoS_2 to form covalent bonds, enabling graphene-electrode devices to maintain relatively stable electrical properties at high temperatures. Therefore, the graphene electrode plays an important role in high-temperature MoS_2 FETs.

We further realized a flexible high-temperature CMOS NOT gate, a basic unit in a logic circuit, by integrating the MoS_2 FET and a h-BN-encapsulated/graphene-electrode WSe_2 FET

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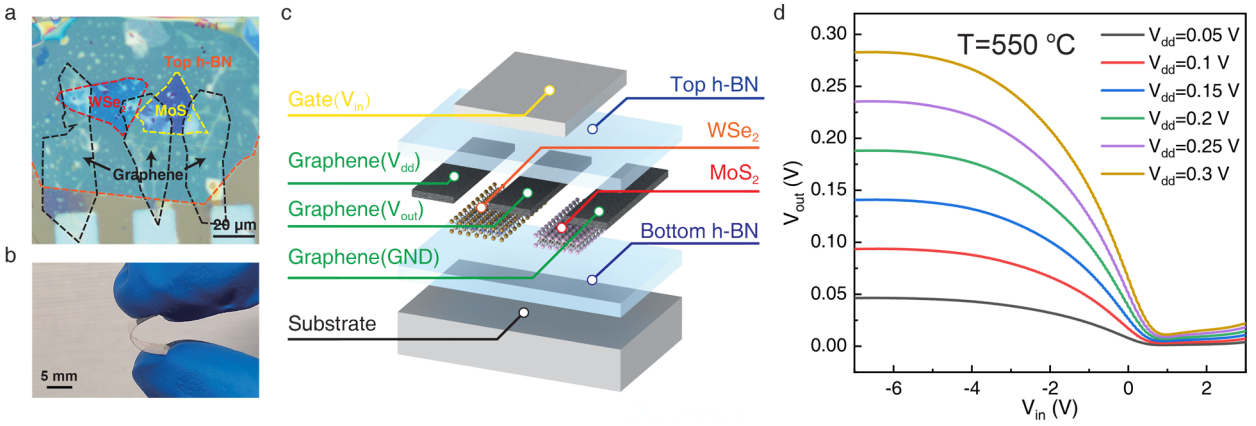

Figure 5. Flexible high-temperature CMOS NOT gate based on a MoS_2 FET and a WSe_2 FET. (a) Optical microscopy image of flexible high-temperature CMOS NOT gate (top gate is not shown). (b, c) Optical image and schematic view of the flexible high-temperature CMOS NOT gate. (d) Voltage transfer curves of the NOT gate measured under 550 °C. As V_{in} is negative (logic "0"), $V_{out} \approx V_{dd}$ (logic "1"). As V_{in} is positive (logic "1"), $V_{out} \approx 0$ V (logic "0").

on a mica substrate (Figure 5a). The device illustrates excellent flexibility (bending radius <5 mm, Figure 5b) and good electrical properties under bending state (Figure S13). As shown in Figure 5c, few-layer WSe_2 flakes and MoS_2 flakes serve as the *p*-channel and the *n*-channel of the NOT gate, respectively, and three graphene electrodes are V_{dd}, V_{out}, and GND, respectively. A Pt universal top gate serves as V_{in}. Figure 5d shows the transfer curves of a representative NOT gate operated at 550 °C. As V_{in} becomes negative (logic "0"), the WSe_2 FET is turned on and the MoS_2 FET is turned off. As a result, V_{dd} mainly distributes on MoS_2 FET and $V_{out} \approx V_{dd}$ (logic "1", V_{dd} ranges from 0.1 to 0.3 V with a 0.05 V step). Conversely, a positive V_{in} (logic "1") turns off the WSe_2 FET and turns on the MoS_2 FET. The V_{dd} mainly distributes on WSe_2 FET and thus $V_{out} \approx 0$ V (logic "0"). Compared with the room-temperature performance (Figure S7 in the Supporting Information), the NOT gate needs a relatively larger ΔV_{in} to switch V_{out} between logic "1" and "0" at 550 °C inasmuch as the SS values of both WSe_2 FET and MoS_2 FET increase under elevated temperature and result in a weaker gating effect.

CONCLUSION

We realized a high-temperature MoS_2 FET with h-BN/h-BN encapsulation and graphene electrodes. With the protection of the h-BN/h-BN structure, the devices can survive at much higher temperature (≥500 °C) than those of state-of-the-art high-temperature MoS_2 devices. Unlike a relatively low-temperature situation, the on/off ratio and subthreshold swing of MoS_2 FET show drastic variation at high temperatures. At high temperatures, carrier mobility still fits the expression $\mu \sim T^{-\gamma}$, suggesting that carrier transportation is limited by phonon scattering. Compared with conventional metal-electrode, devices with a graphene electrode demonstrate superior performance at elevated temperatures (~1 order larger on/off ratio, 3–7 times smaller SS, and 5–9 times smaller threshold voltage shift). We further fabricated a flexible CMOS NOT gate based on MoS_2 FET and WSe_2 FET, and realized logic computing at 550 °C. This work may stimulate the fundamental research of properties of 2D materials at high temperature, and create conditions for next-generation flexible high-performance high-temperature-resistant integrated circuits which can be applied to aerospace, deep drilling, robot working in high-temperature environment, etc.

METHODS

Device Fabrication. We prepared a clean silicon/silicon dioxide (300 nm) substrate and mica substrate by immersing them in acetone, alcohol, and deionized water successively for 2 min of ultrasonic cleaning. We first fabricated 5 nm Ti/30 nm Pt electrodes for graphene contact using photolithography, metal deposition, and the lift-off process. Then, bottom h-BN (30–50 nm), multilayer MoS_2 (5–10 nm), two graphene contacts (5–10 nm), and top h-BN (15–30 nm) were mechanically exfoliated using cellophane tape and transferred onto substrate by PDMS stamp. The h-BN bulk crystals were purchased from SixCarbon Technology Shenzhen. The transfer process was carried out by using an accurate transfer platform (Metatest, E1-T). Finally, a 5 nm Ti/30 nm Pt electrode was fabricated as the top gate. The width of the top gate was 40 μm. The annealing process for as-fabricated devices was carried out in an argon atmosphere at 200 °C for 2 h.

Device Characterizations. The thicknesses of the 2D materials were characterized by atomic force microscopy (AFM) (Bruker, Dimension Icon) using the ScanAsyst-air mode. The Raman spectra were derived by Raman spectrometer (HORIBA Jobin Yvon, LabRAM HR Evolution) with 532 nm laser (0.325 mW/cm^2) and an acquisition time of 120 s. The cross-sectional images of van der Waals heterostructures were characterized by high-resolution transmission electron microscopy (HRTEM) (Model JEOL-2100 TEM, JEOL) with an acceleration voltage of 200 kV. The samples for HRTEM were prepared using a xenon-focused ion beam (Helios G4).

Device Measurements. The electrical characteristics of the MoS_2 FET under different temperatures were measured by a semiconductor parameter analyzer (Agilent, Model B1500A) and a variable-temperature-probe station (Model HCP621G-PM, INSTEC).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.3c13220.

Atomic force microscopy (AFM) image and height-position curve of h-BN; optical images and Raman spectra of MoS_2 flake before and after 500 °C heating for 30 min; optical images of bare, ALD HfO_2 coated, and h-BN encapsulated MoS_2 FET before and after 500 °C heating for 10 min; bubbles occurred on the surface of the metal electrode after 500 °C heating for 10 min; I_{ds}–V_{ds} curves and conductivity (G)–T curves at different gate voltages of graphene-contact device; the process of extracting SBHs of Ti-electrode and Au-electrode

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devices; voltage transfer curves of a NOT gate measured under 25 °C; optical images of bare MoS_2 FET before (a) and after (b) 500 °C heating for 10 min in vacuum; Raman spectrum of MoS_2 from 25 to 500 °C; contact resistance of the device at elevated temperatures and gate voltage; transfer curve of a representative device after heating at 500 °C for 10 min; transfer curves of a representative device at 400 and 500 °C; electrical properties of a representative device under bending state (PDF)

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Author Contributions

P.L. and Z.Y. conceived the experiments. Y.Z. and C.S. fabricated the devices and performed the electrical measurements. J.Y. performed the Raman measurement. H.Z. performed the atomic layer deposition. P.L., Y.Z., C.S., and Z.Z. analyzed the results. P.L. and Y.Z. cowrote the manuscript. All authors discussed the results and commented on the manuscript.

Notes

The authors declare no competing financial interest.

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